Status of the Claims

The listing of claims below will replace all prior versions and listings of claims in the application.

1. (Previously Presented) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a data signal and an origin port configured to produce said data signal; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein a first interconnect of said set of interconnects has a first length, a second interconnect of said set of interconnects has a second length, and said first length and said second length are substantially equal;

wherein said first interconnect is configured to convey a first bit of a number of bits of said data signal and said second interconnect is configured to convey a second bit of said number of bits of said data signal and said first bit remains substantially synchronized with said second bit.

2. (Original) The cross link multiplexer bus of claim 1, wherein said plurality of cross link multiplexers are arranged in a substantially circular configuration.

3. (Original) The cross link multiplexer bus of claim 1, wherein said plurality of cross link multiplexers are arranged in a substantially spherical configuration.

4. (Original) The cross link multiplexer bus of claim 1, wherein a cross link multiplexer of said plurality of cross link multiplexers comprises a cross link multiplexer pair.

5. (Previously Presented) The cross link multiplexer bus of claim 1, wherein:

said data signal is configured to be represented as a series of characters, and a character of said series of characters is configured to be represented as said number of bits.

6. (Canceled)

7. (Previously Presented) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a data signal, at least one delay buffer configured to delay conveyance of said data signal, and an origin port configured to produce said data signal; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein a first interconnect of said set of interconnects is configured to convey a first bit of a number of bits of said data signal and a second interconnect of said set of interconnects is configured to convey a second bit of said number of bits of said data signal and said first bit remains substantially synchronized with said second bit.

8. (Previously Presented) The cross link multiplexer of claim 7, wherein:

said data signal is configured to be represented as a series of characters, and a character of said series of characters is configured to be represented as said number of bits.

9. (Previously Presented) The cross link multiplexer bus of claim 7, wherein said at least one delay buffer is a series of delay buffers.

10. (Previously Presented) The cross link multiplexer bus of claim 9, wherein said series of delay buffers is configured to convey said first bit through said delay buffer and is configured to bypass said first bit around said delay buffer.

11. (Previously Presented) The cross link multiplexer bus of claim 10, wherein said cross link multiplexer has a control circuit, said control circuit configured to align said series of delay buffers to be configured to convey said first bit through said delay buffer or to bypass said first bit around said delay buffer.

12. (Previously Presented) The cross link multiplexer of claim 11, wherein said control circuit is configured to align said series of delay buffers so that said first bit remains substantially synchronized with said second bit.

13. (Previously Presented) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a first cross link multiplexer with a destination port configured to receive a data signal and a second cross link multiplexer with an origin port configured to produce said data signal; and

a plurality of interconnects, wherein a first set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein a first interconnect of said first set of interconnects is configured to convey a first bit of a number of bits of said data signal in a first direction and a second interconnect of said first set of interconnects is configured to convey a second bit of said number of bits of said data signal in said first direction;

wherein said first cross link multiplexer is configured to convey said data signal toward said second cross link multiplexer in said first direction via said first set of interconnects coupled to a third cross link multiplexer of said plurality of cross link multiplexers and said first cross link multiplexer is configured to convey said data signal toward said second cross link multiplexer in a second direction via a second set of interconnects of said plurality of interconnects coupled other than to said third cross link multiplexer.

14-16. (Canceled)

17. (Previously Presented) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a data signal and an origin port configured to produce said data signal; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein said data signal is configured to be represented as a series of characters, and a character of said series of characters is configured to be represented as a number of bits;

wherein a first interconnect of said set of interconnects is configured to convey a first bit of said number of bits of said data signal in a direction and a second interconnect of said set of interconnects is configured to convey a second bit of said number of bits of said data signal in said direction;

wherein at least one of said plurality of cross link multiplexers and said plurality of interconnects is configured so that said first bit remains substantially synchronized with said second bit.

18. (Previously Presented) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a signal and an origin port configured to produce said signal; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein said signal is configured to be represented as a series of characters, and a character of said series of characters is configured to be represented as a number of bits;

wherein at least one of said plurality of cross link multiplexers and said plurality of interconnects is configured so that a first bit of said number of bits remains substantially synchronized with a second bit of said number of bits;

wherein said plurality of cross link multiplexers is configured to delay conveyance of said first bit by a gate delay time;

wherein said plurality of interconnects is configured to delay conveyance of said second bit by a path delay time; and

wherein said gate delay time and said path delay time are set so that said first bit remains substantially synchronized with said second bit.

19. (Previously Presented) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a signal and an origin port configured to produce said signal; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein said signal is configured to be represented as a series of characters, and a character of said series of characters is configured to be represented as a number of bits;

wherein at least one of said plurality of cross link multiplexers and said plurality of interconnects is configured so that a first bit of said number of bits remains substantially synchronized with a second bit of said number of bits; and

wherein a first cross link multiplexer of said plurality of cross link multiplexers is configured to process said signal formatted according to a first physical layer communications protocol and a second cross link multiplexer of said plurality of cross link multiplexers is configured to process said signal formatted according to a second physical layer communications protocol.

20. (Original) The cross link multiplexer bus of claim 19, wherein said first physical layer communications protocol is a 10 Gigabit Media Independent Interface protocol.

21. (Original) The cross link multiplexer bus of claim 19, wherein said second physical layer communications protocol is a 10 Gigabit Attachment Unit Interface protocol.

22. (Original) The cross link multiplexer bus of claim 19, wherein said second physical layer communications protocol is a Converged Data Link protocol.

23. (Original) The cross link multiplexer bus of claim 19, wherein said first cross link multiplexer is configured to reformat said signal formatted according to said first physical layer communications protocol.

24. (Previously Presented) A method for conveying a data signal across a cross link multiplexer bus, comprising the steps of:

(1) conveying the data signal from a first cross link multiplexer of the cross link multiplexer bus via a second cross link multiplexer of the cross link multiplexer bus toward a third cross link multiplexer of the cross link multiplexer bus; and

(2) conveying the data signal from the first cross link multiplexer other than via the second cross link multiplexer toward the third cross link multiplexer;

wherein a first interconnect of a plurality of interconnects is used to convey a first bit of the data signal from the first cross link multiplexer to the second cross link multiplexer and a second interconnect of the plurality of interconnects is used to convey a second bit of the data signal from the first cross link multiplexer to the second cross link multiplexer.

25. (Previously Presented) The method of claim 24, further comprising the step of:

(3) receiving the data signal at the first cross link multiplexer.

26-28. (Canceled)

29. (Previously Presented) The method of claim 24, further comprising the step of:

(3) transmitting the data signal from the third cross link multiplexer.

30. (Previously Presented) A method for conveying, in parallel, bits of a character of a data signal across a cross link multiplexer bus, comprising the steps of:

(1) conveying a first bit of the bits of the character of the data signal from a first cross link multiplexer of the cross link multiplexer bus to a second cross link multiplexer of the cross link multiplexer bus;

(2) conveying a second bit of the bits of the character of the data signal from the first cross link multiplexer to the second cross link multiplexer; and

(3) delaying said conveyance of the first bit so that the first bit remains substantially synchronized with the second bit.

31. (Original) The method of claim 30, wherein said delaying step comprises the step of conveying the first bit through a delay buffer.

32. (Previously Presented) A method for conveying a signal across a cross link multiplexer bus, comprising the steps of:

(1) conveying the signal from a first cross link multiplexer of the cross link multiplexer bus to a second cross link multiplexer of the cross link multiplexer bus; and

(2) at one of the first cross link multiplexer and the second cross link multiplexer, converting the signal from a first format to a second format;

(3) synchronizing bits of a character of the signal;

wherein the first format is one of a 10 Gigabit Media Independent Interface protocol, a 10 Gigabit Attachment Unit Interface protocol, and a Converged Data Link protocol, the second format is one of the 10 Gigabit Media Independent Interface protocol, the 10 Gigabit Attachment Unit Interface protocol, and the Converged Data Link protocol, and the second format is different from the first format.

33. (Previously Presented) The method of claim 32, further comprising the step of:

(4) receiving the signal at the first cross link multiplexer.

34. (Previously Presented) The method of claim 32, further comprising the step of:

(4) reconverting the signal from the second format to the first format.

35. (Previously Presented) The method of claim 32, further comprising the step of:

(4) transmitting the signal from the second cross link multiplexer.

36. (Canceled)

37. (Previously Presented) A method for conveying a signal across a cross link multiplexer bus, comprising the steps of:

(1) conveying the signal from a first cross link multiplexer of the cross link multiplexer bus to a second cross link multiplexer of the cross link multiplexer bus;

(2) at one of the first cross link multiplexer and the second cross link multiplexer, converting the signal from a first format to a second format; and

(3) synchronizing bits of a character of the signal;

wherein said synchronizing step comprises the step of conveying each bit of the bits through a corresponding delay flip-flop.

38. (Original) The method of claim 37, wherein said synchronizing step further comprises the step of conveying a bit of the bits through a delay buffer.

39. (Previously Presented) A method for conveying a signal across a cross link multiplexer bus, comprising the steps of:

(1) conveying the signal from a first cross link multiplexer of the cross link multiplexer bus to a second cross link multiplexer of the cross link multiplexer bus;

(2) at one of the first cross link multiplexer and the second cross link multiplexer, converting the signal from a first format to a second format; and

(3) synchronizing bits of a character of the signal;

wherein the signal is configured to be represented as a series of characters;

wherein one character of the series of characters is conveyed during one cycle of a clock that controls conveyance of the signal;

wherein the first format has a first number of bits for data for a first character from the series of characters; and

wherein the second format has a second number of bits for data for the first character and data for a second character from the series of characters.

40. (Original) The method of claim 39, wherein said converting step comprises the steps of:

(a) during a first cycle of the clock, conveying the first character from an input of a first interconnect to an output of the first interconnect;

(b) during the first cycle of the clock, conveying the first character from an input of a second interconnect to a delay flip-flop;

(c) during a second cycle of the clock, conveying the second character from the input of the first interconnect to the output of the first interconnect; and

(d) during the second cycle of the clock, conveying the first character from the delay flip-flop to an output of the second interconnect.

41. (Previously Presented) In a cross link multiplexer bus configured to convey a data signal in which a character is represented by a first bit and a second bit, a method for synchronizing the first bit and the second bit, comprising the steps of:

(1) determining a first time for the first bit of the data signal to be conveyed via a first interconnect from a first cross link multiplexer to a second cross link multiplexer when a first series of delay buffers is bypassed;

(2) determining a second time for the second bit of the data signal to be conveyed via a second interconnect from the first cross link multiplexer to the second cross link multiplexer when a second series of delay buffers is bypassed, the second time greater than the first time;

(3) determining a desired delay time for the first bit of the data signal so that the first bit of the data signal is synchronized with the second bit of the data signal; and

(4) aligning the first series of delay buffers to increase the first time by the desired delay time so that the first bit of the data signal is synchronized with the second bit of the data signal.

42. (Previously Presented) The method of claim 41, wherein said aligning step comprises the step of configuring the first series of delay buffers so that the first bit of the data signal is conveyed through a first delay buffer of the first series of delay buffers.

43. (Previously Presented) In a cross link multiplexer bus configured to convey a signal in which a character is represented by a first bit and a second bit, a method for synchronizing the first bit and the second bit, comprising the steps of:

(1) determining a first time for the first bit to be conveyed via a first interconnect from a first cross link multiplexer to a second cross link multiplexer when a first series of delay buffers is bypassed;

(2) determining a second time for the second bit to be conveyed via a second interconnect from the first cross link multiplexer to the second cross link multiplexer when a second series of delay buffers is bypassed, the second time greater than the first time;

(3) determining a desired delay time for the first bit so that the first bit is synchronized with the second bit; and

(4) aligning the first series of delay buffers to increase the first time by the desired delay time so that the first bit is synchronized with the second bit;

wherein said aligning step comprises the steps of:

configuring the first series of delay buffers so that the first bit is conveyed through a first delay buffer of the first series of delay buffers; and

configuring the first series of delay buffers so that the first bit bypasses a second delay buffer of the first series of delay buffers.